

|  |
| --- |
| Group 2 |
| CST 2540 Group Coursework 2 G9 |
|  |

|  |
| --- |
|  |

## Amal Ali Anwar M00734729

## Mirza Mohammad Faiq Baig M00696479

## Hamad Mohamed Asif M00695912

## **Tutor: Madhumita Das**

## **Module Leader: Dr Purav Shah**

14th April 2021

**INDIVIDUAL TASKS:**

**2.** Following are non-valid BCD encodings for the decimal digits:

* 1010
* 1011
* 1100
* 1101
* 1111

|  |  |
| --- | --- |
| State | Description |
| *S0* | *The 3 most recent bits are x00* |
| *S1* | *The 3 most recent bits are 001* |
| *S2* | *The 3 most recent bits are 010* |
| *S3* | *The 3 most recent bits are 011* |
| *S4* | *The 3 most recent bits are 101* |
| *S5* | *The 3 most recent bits are 110* |
| *S6* | *The 3 most recent bits are 111* |

The state machines would need to detect when the significant bits would be 101 or 11. The table below would define the states.

*Table 1*

I will use the states defined above and obtain the *Next State (N.S)* and the *Output (Z)* for the *Present State* and the *Input (X).*

Consider the *present state* as *S0*,

If the input is 1, then the *next state* is *S1* and the output is *Z = 0*.

If the input is 0, then the *next state* is *S0*and the output is *Z = 0.*

Consider the *present state* as *S1*,

If the input is 1, then the *next state* is *S3* and the output is *Z = 0.*

If the input is 1, then the *next state* is *S2* and the output is *Z = 0.*

Consider the *present state* as *S2*,

If the input is 1, then the *next state* is *S4* and the output is *Z = 0.*

If the input is 1, then the *next state* is *S0* and the output is *Z = 0.*

Consider the *present state* as *S3*,

If the input is 1, then the *next state* is *S6* and the output is *Z = 0.*

If the input is 1, then the *next state* is *S5* and the output is *Z = 0.*

Consider the *present state* as *S4*,

If the input is 1, then the *next state* is *S3* and the output is *Z = 1.*

If the input is 1, then the *next state* is *S2* and the output is *Z = 1.*

Consider the *present state* as *S5*,

If the input is 1, then the *next state* is *S4* and the output is *Z = 1.*

If the input is 1, then the *next state* is *S0* and the output is *Z = 1.*

Consider the *present state* as *S6*,

If the input is 1, then the *next state* is *S6* and the output is *Z = 1.*

If the input is 1, then the *next state* is *S5* and the output is *Z = 1.*

Using the explanation, below is the state table for the *Mealy Sequential circuit*:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| *Present State* | *Next State* | | | *Output* | |
|  | *X = 0*  *X = 1* | | | *X = 0*  *X =1* | |
| *S0* | *S1* | *S1* | 0 | | 0 |
| *S1* | *S2* | *S3* | 0 | | 0 |
| *S2* | *S0* | *S4* | 0 | | 0 |
| *S3* | *S5* | *S6* | 0 | | 0 |
| *S4* | *S2* | *S3* | 1 | | 1 |
| *S5* | *S0* | *S4* | 1 | | 1 |
| *S6* | *S5* | *S6* | 1 | | 1 |

**3.** The initial state, or reset state, is when neither the button has been pushed nor is Z high. This is S0. The next state would be S1, where the button is pushed and X is high, and Z is high for its first clock cycle. S2 would be Z’s second clock cycle while it is high. S3 would be its third, and S4 would be the fourth and final clock cycle where Z is high. During all 4 of Z’s high states, X is a don’t-care since Z remains high for these 4 states regardless of what X’s value is. S5 is where X is still 1 and Z returns to low, and the machine remains in this state as long as X stays pressed after Z is done with its clock cycles. Upon X going back to low (which means the button is no longer being pressed), the machine enters the reset state where X and Z are both low. Below is the state graph:

